#16/RCE

1-23-02 Sudlow

UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	KAO et al.	Docket No:	16405-0311
Serial No:	09/256,265	Group Art Unit	2815
Filing Date:	February 23, 1999	Examiner:	Diaz, J.

Title: **"METHOD AND APPARATUS FOR SPLIT GATE SOURCE SIDE INJECTION FLASH MEMORY CELL AND ARRAY WITH DEDICATED ERASE GATES"**

Box RCE
Assistant Commissioner for Patents
Washington, D.C. 20231

REQUEST FOR CONTINUED EXAMINATION (RCE) UNDER 37 CFR 1.114 AND PRELIMINARY AMENDMENT

Sir:

Applicants are submitting this amendment along with a Request for Continued Examination (RCE) under 37 CFR 1.114. Please amend the above identified application as follows and consider the following remarks in response to the Advisory Action mailed on October 10, 2001 and the Final Office Action mailed on July 18, 2001 for the above identified prior application.

In The Claims

1. (Twice Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region defined thereon;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate generally disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a portion of said substrate and being separated therefrom by said second insulating layer, a second portion formed over a first one of